AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A semiconductor memory device comprising:

a first conductivity type semiconductor substrate; ~~and~~

a plurality of memory cells each comprising ~~constituted of~~ an island-like semiconductor layer which is formed on the semiconductor substrate, and a charge storage layer and a control gate which are formed entirely or partially around a sidewall of the island-like semiconductor layer,

wherein the plurality of memory cells are disposed in series, and for at least one of the island-like semiconductor layers the island-like semiconductor layer ~~which constitutes the memory cells~~ has different cross-sectional widths ~~areas~~ varying in stages so as to have different widths at different distances from the semiconductor substrate ~~in a horizontal direction of the semiconductor substrate~~, and

an insulating film capable of passing charges is provided at least in a part of a plane of the island-like semiconductor layer horizontal to the semiconductor substrate.

2. (Original) The device according to claim 1, wherein the cross-sectional areas of the island-like semiconductor layer are step by step small to the direction of the surface of the semiconductor substrate.

3. (Original) The memory device according to claim 1, wherein the cross-sectional areas of the island-like semiconductor layer are step by step large to the direction of the surface of the semiconductor substrate.

4. (Original) The device according to claim 1, wherein the cross-sectional area of the island-like semiconductor layer distant from the semiconductor substrate is equal to that of the island-like semiconductor layer close to the semiconductor substrate.

5. (Original) The device according to claim 1, wherein the island-like semiconductor layer involves at least two same sizes of the cross-sectional areas thereof.

6. (Original) The device according to claim 1, wherein the plurality of memory cells are electrically insulated from the semiconductor substrate by a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the island-like semiconductor layer, or by both of said second conductivity type impurity diffusion layer and a first conductivity type impurity diffusion layer formed in the second conductivity type impurity diffusion layer.

7. (Original) The device according to claim 1, wherein at least one of the memory cells is electrically insulated from another memory cell by a second conductivity type impurity diffusion layer formed in the island-like semiconductor layer, or by both said second conductivity type impurity diffusion layer and a first conductivity type impurity diffusion layer formed in the second conductivity type impurity diffusion layer.

8. (Original) The device according to claim 6, wherein at least one of the memory cells is electrically insulated from another memory cell by a depletion layer formed at a junction of the second conductivity type impurity diffusion layer in the semiconductor substrate or the island-like semiconductor layer.

9. (Original) The device according to claim 7, wherein at least one of the memory cells is electrically insulated from another memory cell by a depletion layer formed at a junction of the second conductivity type impurity diffusion layer in the semiconductor substrate or the island-like semiconductor layer.

10. (Original) The device according to claim 1, wherein an impurity diffusion layer is formed on the surface of the semiconductor substrate and serves as common wiring of the memory cells.

11. (Original) The device according to claim 1, wherein a plurality of said island-like semiconductor layers are arranged in matrix, wiring for reading out the state of a charge stored in the memory cells is formed in the island-like semiconductor layers, a plurality of the control gates are disposed continuously in one direction so as to form a control gate line, and a plurality of wirings in a direction crossing the control gate line are connected to form a bit line.

12. (Original) The device according to claim 1, wherein a gate electrode for selecting the memory cells formed entirely or partially around the sidewall of the island-like semiconductor

layer is formed at least on one end of the island-like semiconductor layer and the gate electrode is disposed in series with the memory cells.

13. (Original) The device according to claim 11, wherein the island-like semiconductor layer opposed to the gate electrode is electrically insulated from the semiconductor substrate or the memory cells by a second conductivity type impurity diffusion layer formed in the surface of the semiconductor substrate or the island-like semiconductor layer.

14. (Original) The device according to claim 11, wherein a second conductivity type impurity diffusion layer, or the second conductivity type impurity diffusion layer and a first conductivity type impurity diffusion layer formed therein is/are formed, in self-alignment with the charge storage layer, in a part or the entirety of respective corners of the island-like semiconductor layer having a step shape so that channel layers of memory cells are electrically connected to each other.

15. (Original) The device according to claim 11, wherein a second conductivity type impurity diffusion layer, or the second conductivity type impurity diffusion layer and a first conductivity type impurity diffusion layer formed therein is/are formed, in self-alignment with the charge storage layer and the gate electrode, in a part or the entirety of respective corners of the island-like semiconductor layer having a step shape so that a channel layer of at least one memory cell and another channel layer which is disposed in the island-like semiconductor layer and opposed to the gate electrode are electrically connected.

16. (Original) The device according to claim 1, wherein a plurality of said control gates are disposed close to each other so that channel layers of the memory cells are electrically connected.

17. (Original) The device according to claim 11, wherein the control gate and the gate electrode are disposed close to each other so that a channel layer of at least one memory cell and another channel layer which is disposed in the island-like semiconductor layer and opposed to the gate electrode are electrically connected.

18. (Original) The device according to claim 1, further comprising an electrode between the control gates for electrically connecting channel layers of the memory cells.

19. (Original) The device according to claim 11, further comprising an electrode between the control gate and the gate electrode for electrically connecting a channel layer of at least one memory cell and another channel layer which is disposed in the island-like semiconductor layer and opposed to the gate electrode.

20. (Original) The device according to claim 11, wherein the control gate and a part or the entirety of the gate electrode are made of the same material.

21. (Original) The device according to claim 11, wherein the charge storage layer and the gate electrode are made of the same material.

22. (Original) The device according to claim 1, wherein a plurality of said island-like semiconductor layers are arranged in matrix and the width of the island-like semiconductor layers in one direction is narrower than the distance between the adjacent island-like semiconductor layers in the same direction.

23. (Original) The device according to claim 1, wherein a plurality of said island-like semiconductor layers are arranged in matrix and the distance between the island-like semiconductor layers in one direction is shorter than that between the island-like semiconductor layers in a different direction.

24-32. (Canceled)